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EXAMINER	
OCHOA, JUAN CARLOS	
ART UNIT	**PAPER NUMBER**
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,612	NAHAS, JOSEPH J.	
	Examiner	Art Unit	
	Juan C. Ochoa	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1–41 are presented for examination.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because:

3. As to Figure 5, it includes the following reference character(s) not mentioned in the description: 503 and 505.

4. As to Figure 11, it includes the following reference character(s) not mentioned in the description: 1103, 1105, and 1107.

5. As to Figure 19, it includes the following reference character(s) not mentioned in the description: 1919.

6. Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

7. The specification is objected to because of the following informalities:

8. In page 5, paragraph [0031], line 3, "2223" should be 223.

9. In page 8, paragraph [0040], equation (6), "E_rE_o" should be $\varepsilon_r\varepsilon_o$.

10. Appropriate correction is required.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. Claims 1, 16, 29, and 41 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted step is:

13. Failure to specify the MRAM's read or write mode.

14. Dependent claims 2–15, 17–28, and 30–40 inherit the defect of the claims from which they depend.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1–4, 6, 12–14, 29–31, 33, 37, and 39–41 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al., (Kim hereinafter), Macro Model and Sense Amplifier for a MRAM.

17. As to claim 1, Kim discloses a method for simulating a magneto resistive memory device of a magneto resistive random access memory (MRAM) having a first conductor, a second conductor, and a magnetic tunnel junction (MTJ), the first conductor disposed substantially orthogonal to the second conductor, the MTJ disposed between the first conductor and the second conductor, the method comprising: calculating a first and a second current in the first and second conductor (see page 898, col. 1, last two lines and col. 2, lines 1–8); detecting an indication of a transition of one of the first current and the second current across a threshold (see page 899, col. 1, lines 6–15); modifying a status of an operating condition of a plurality of operating conditions in response to the detecting the indication of the transition (see page 899, col. 1, lines 15–20); and outputting a bit state that is dependent upon a status of the plurality of operating conditions (see page 899, col. 1, lines 3–6).

18. As to claim 2, Kim discloses a method further comprising: calculating a current conducted through the MTJ based on a logic value of the bit state (see page 899, col. 1, lines 25–30).

19. As to claim 3, Kim discloses a method further comprising: modeling a conductance value of the MTJ in each of two bit states using an equation having an equivalent form of $G(A+BV+CV^2)$, where G is a conductance value of the MTJ, A, B,

and C are zero, first, and second order voltage coefficient parameters, and V is a MTJ bias voltage value (see page 899, col. 2, lines 6–12).

20. Claim 3 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 899, col. 2, lines 6–12) is functionally equivalent to the results produced by the step expressly claimed in Applicant's dependent claim 3. Therefore, the "product" that is produced by performing the step disclosed in dependent claim 8 is the functional equivalent of the "product" that is produced in (page 899, col. 2, lines 6–12). Although the "step" by which the end result is different, the final result for the "step" is identical.

21. As to claim 4, Kim discloses a method utilizing a first set of zero, first, and second order voltage coefficient parameters for the conductance value for a first bit state and utilizing a second set of, zero, first, and second order voltage coefficient parameters for the conductance value for a second bit state (see page 899, col. 2, lines 6–12).

22. Claim 4 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 899, col. 2, lines 6–12) is functionally equivalent to the results produced by the step expressly claimed in Applicant's dependent claim 4. Therefore, the "product" that is produced by performing the step disclosed in dependent claim 8 is the functional equivalent of the "product" that is produced in (page 899, col. 2, lines 6–12). Although the "step" by which the end result is different, the final result for the "step" is identical.

23. As to claim 6, Kim discloses a method further comprising: calculating A, B, and C as a function of temperature (see page 899, col. 2, lines 6–12).

24. As to claim 12, Kim discloses a method wherein the detecting an indication of a transition of one of the first current and the second current across a threshold, further includes: calculating a first magnetic field from the first current; calculating a second magnetic field from the second current; detecting a transition of one of the first magnetic field and the second magnetic field across a threshold (see page 899, col. 1, lines 20–25).

25. Claim 12 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 899, col. 1, lines 20–25) is functionally equivalent to the results produced by the step expressly claimed in Applicant's dependent claim 12. Therefore, the "product" that is produced by performing the step disclosed in dependent claim 8 is the functional equivalent of the "product" that is produced in (page 899, col. 1, lines 20–25). Although the "step" by which the end result is different, the final result for the "step" is identical.

26. As to claim 13, Kim discloses a method wherein the plurality of operating conditions include a condition indicative of a presence of a current in the first conductor above a predetermined threshold (see page 899, col. 1, lines 11–15).

27. As to claim 14, Kim discloses a method wherein the threshold is a first threshold corresponding to the first current exceeding a lower threshold while increasing (see page 899, col. 1, lines 9–15).

28. As to claim 29, Kim discloses a method for simulating a magneto resistive memory device in an integrated circuit magneto resistive random access memory (MRAM) having a first conductor, a second conductor, and a magnetic tunnel junction (MTJ), the first conductor disposed substantially orthogonal to the second conductor, the MTJ disposed between the first conductor and the second conductor, the method comprising: calculating an indication of a first magnetic field applied to the MTJ, the first magnetic field generated by current in the first conductor; calculating an indication of a second magnetic field applied to the MTJ, the second magnetic field generated by current in the second conductor (see page 898, col. 1, last two lines and col. 2, lines 1–8); detecting indications of transitions of the first magnetic field and the second magnetic field across one or more thresholds (see page 899, col. 1, lines 6–15); and providing a state machine having one or more state variables with transitions in the state machine being dependent upon detected indications of transitions of the first magnetic field and the second magnetic field and a state of the one or more state variables (see page 899, col. 1, lines 3–6).

29. As to claim 30, Kim discloses a method further comprising: modeling a conductance value of the MTJ in each of two bit states using an equation having an equivalent form of $G(A+BV+CV^2)$, where G is a conductance value of the MTJ, A, B, and C are zero, first, and second order voltage coefficient parameters, and V is a MTJ bias voltage value (see page 899, col. 2, lines 6–12).

30. Claim 30 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 899, col. 2, lines 6–12) is functionally

equivalent to the results produced by the step expressly claimed in Applicant's dependent claim 30. Therefore, the "product" that is produced by performing the step disclosed in dependent claim 8 is the functional equivalent of the "product" that is produced in (page 899, col. 2, lines 6–12). Although the "step" by which the end result is different, the final result for the "step" is identical.

31. As to claim 31, Kim discloses a method utilizing a first set of zero, first, and second order voltage coefficient parameters for the conductance value for a first bit state and utilizing a second set of, zero, first, and second order voltage coefficient parameters for the conductance value for a second bit state (see page 899, col. 2, lines 6–12).

32. Claim 31 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 899, col. 2, lines 6–12) is functionally equivalent to the results produced by the step expressly claimed in Applicant's dependent claim 31. Therefore, the "product" that is produced by performing the step disclosed in dependent claim 8 is the functional equivalent of the "product" that is produced in (page 899, col. 2, lines 6–12). Although the "step" by which the end result is different, the final result for the "step" is identical.

33. As to claim 33, Kim discloses a method further comprising: calculating A, B, and C as a function of temperature (see page 899, col. 2, lines 6–12).

34. As to claim 37, Kim discloses a method wherein state variables of the state machine is a state variable indicative of a presence of the first magnetic field above a predetermined threshold (see page 899, col. 1, lines 9–15).

35. As to claim 39, Kim discloses a method wherein the threshold is a first threshold corresponding to the first magnetic field exceeding a lower threshold while increasing (see page 899, col. 1, lines 9–15).

36. As to claim 40, Kim discloses a method wherein the calculating an indication of a first magnetic field applied to the MTJ further includes calculating a first current in the first conductor; the calculating an indication of a second magnetic field applied to the MTJ further includes calculating a second current in the second conductor (see page 899, col. 1, lines 20–25).

37. Claim 40 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 899, col. 1, lines 20–25) is functionally equivalent to the results produced by the step expressly claimed in Applicant's dependent claim 40. Therefore, the "product" that is produced by performing the step disclosed in dependent claim 8 is the functional equivalent of the "product" that is produced in (page 899, col. 1, lines 20–25). Although the "step" by which the end result is different, the final result for the "step" is identical.

38. As to claim 41, this claim recites a computer readable medium having stored instructions for performing the method of claim 1. Kim discloses an a HSPICE macro–model (see page 901, col. 1, last paragraph, lines 6–7) for performing a method that anticipates claim 1 and, therefore claim 41 is rejected for the same reasons given above.

Claim Rejections - 35 USC § 103

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. The factual inquiries set forth in Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

41. Claims 5 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim as applied to claims 3 and 30 above, taken in view of Bodhisattva Das and William C. Black, (Das hereinafter), A Generalized HSPICE™ Macro-Model for Pinned Spin-Dependent-Tunneling Devices.

42. As to claims 5 and 32, while Kim discloses a method for simulating an MTJ MRAM modeling a conductance value of the MTJ in each of two bit states, Kim fails to disclose utilizing a first set of coefficients for the conductance value for a positive MTJ bias voltage and utilizing a second set of coefficients for the conductance value for a negative MTJ bias voltage, in at least one of the two bit states.

43. Das discloses utilizing a first set of coefficients for the conductance value for a positive MTJ bias voltage and utilizing a second set of coefficients for the conductance

value for a negative MTJ bias voltage, in at least one of the two bit states. (See page 2890, col. 1, lines 18–22).

44. Claims 5 and 32 have been given a broad reasonable interpretation by the Examiner. The Examiner notes that the process disclosed in Das (page 2890, col. 1, lines 18–22) is functionally equivalent to the results produced by the steps expressly claimed in Applicant's independent claims 5 and 32. Therefore, the "product" that is produced by performing the steps disclosed in independent claims 5 and 32 is the functional equivalent of the "product" that is produced in Das (page 2890, col. 1, lines 18–22). Although the "process" by which the end result is different, the final result for the "process" is identical.

45. Kim and Das are analogous art because they are both related to computer model simulations for MTJ MRAM cells.

46. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the method of Das in the method of Kim because Das models the quasi-static hysteretic nature and thermal effects of an SDT device (see page 2889, col. 1, lines 25–28), and as a result, Das improves over his previous model for different types of giant magneto resistance (GMR) memory bits. (See page 2889, col. 1, lines 28–30).

47. Claims 7, 15, and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim as applied to claims 1, 3 and 30 above, taken in view of Maxim et al., (Maxim

hereinafter), A Novel Behavioral Method of SPICE Macro–modeling of Magnetic Components Including the Temperature and Frequency Dependencies.

48. As to claim 7, while Kim discloses a method for simulating an MTJ MRAM modeling a conductance value of the MTJ in each of two bit states, Kim fails to disclose a method wherein values of G, A, B, and C are generated by fitting low resistance state conductance data, high resistance state conductance negative bias voltage data, and high resistance state conductance positive bias voltage data for predetermined temperatures with second order polynomials; and fitting individual polynomial coefficient parameters to first order temperature polynomials.

49. Maxim discloses a method wherein values of G, A, B, and C are generated by a method comprising: fitting low resistance state conductance data, high resistance state conductance negative bias voltage data, and high resistance state conductance positive bias voltage data for predetermined temperatures with second order polynomials (see page 396, col. 1, lines 29–34); and fitting individual polynomial coefficient parameters to first order temperature polynomials (see page 397, col. 1, lines 3–14).

50. Maxim and Kim are analogous art because they are both related to macro–modeling of magnetic components.

51. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the Macro–modeling of Maxim in the method of Kim because Maxim achieves portability of his macro–model to SPICE simulators that do not support time integral (SDT) and time derivative (DDT) predefined ABM functions (see page 398, col. 2, lines 4–7), and as a result, Maxim reports a high computational

efficiency with no convergence problems (see page 399, col. 1, last paragraph, lines 1–4).

52. As to claim 15, Maxim discloses a method of SPICE macro–modeling of magnetic components for simulating wherein the calculating the first current and the calculating the second current are performed during each time step of a simulation of an MRAM memory (see page 398, col. 2, lines 8–16).

53. As to claim 34, Maxim discloses a method wherein values of G, A, B, and C are generated by a method comprising: fitting low resistance state conductance data, high resistance state conductance negative bias voltage data, and high resistance state conductance positive bias voltage data for predetermined temperatures with second order polynomials (see page 396, col. 1, lines 29–34); and fitting individual polynomial coefficient parameters to first order temperature polynomials (see page 397, col. 1, lines 3–14).

54. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim taken in view of Maxim as applied to claim 7 above, and further in view of Peter Lancaster and Kestutis Salkauskas, (Lancaster hereinafter), Curve And Surface Fitting: An Introduction.

55. As to claim 8, while the Kim–Maxim method models coefficients generated by fitting, the Kim–Maxim method fails to disclose using one of a root mean square error or a weighted root mean square error in performing the fitting.

56. Lancaster discloses using one of a root mean square error in performing the fitting (see page 45, next to last paragraph). It is known in the art that least-squares fit is compatible to root-mean square error minimization, when fitting a curve to a set of data.

57. Kim, Maxim, and Lancaster are analogous art because they are related to curve fitting.

58. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the root mean square error of Lancaster in the Kim–Maxim method because, when fitting a curve, Lancaster minimizes the sum of squared deviations (see page 44, last paragraph, lines 1–3), and as a result, Lancaster reports using a simpler function (see page 44, last paragraph, lines 8–9).

59. Claims 9, 11, 35, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim taken in view of Maxim as applied to claims 7 and 34 above, and further in view of Dimopoulos, (Dimopoulos hereinafter), Transport Polarisé En Spin Dans Les Jontions Tunnel Magnétiques: Le Rôle Des Interfaces Métal/Oxyde Dans Le Processus Tunnel.

60. As to claims 9 and 35, while the Kim–Maxim method simulates an MTJ MRAM modeling a conductance value of the MTJ in each of two bit states, the Kim–Maxim method fails to adjust one or more of the individual polynomial coefficient parameters to minimize a total error being measured between the second order polynomials and each of the low resistance state conductance data, the high resistance state conductance

negative bias voltage data, and the high resistance state conductance positive bias voltage data.

61. Dimopoulos discloses adjusting one or more of the individual polynomial coefficient parameters to minimize a total error being measured between the second order polynomials and each of the low resistance state conductance data, the high resistance state conductance negative bias voltage data, and the high resistance state conductance positive bias voltage data (see page 146, Eq. 5.17; pages 152–154; page 160, lines 17–26; and page 161, line 1).

62. Kim, Maxim and Dimopoulos are analogous art because they are related to magnetic tunnel junctions.

63. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the error minimization of Dimopoulos in the Kim–Maxim method because Dimopoulos fits experimental conductance curves for magnetic tunnel junctions (see page 160, lines 4–6), and as a result, Dimopoulos reports that his model describes accurately experimental data for the conductance of magnetic tunnel junctions accounting for observed temperature variations (see page 161, lines 6–9).

64. As to claims 11 and 36, Maxim discloses a eliminating one or more of the polynomial coefficient parameters, which have a minimal effect on error being measured (see page 397, col. 1, next to last paragraph, lines 2 and 5–8).

65. Claims 11 and 36 have been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 397, col. 1, next to last paragraph, lines 2 and 5–8) is functionally equivalent to the results produced by the step

expressly claimed in Applicant's dependent claims 11 and 36. Therefore, the "product" that is produced by performing the step disclosed in dependent claims 11 and 36 is the functional equivalent of the "product" that is produced in (page 397, col. 1, next to last paragraph, lines 2 and 5–8). Although the "step" by which the end result is different, the final result for the "step" is identical.

66. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim taken in view of Maxim further in view of Dimopoulos as applied to claim 9 above, and further in view of Lancaster.

67. As to claim 10, while the Kim–Maxim–Dimopoulos method models coefficients generated by fitting, the Kim–Maxim–Dimopoulos method fails to disclose using one of a root mean square error or a weighted root mean square error in performing the fitting.

68. Lancaster discloses using one of a root mean square error in performing the fitting (see page 45, next to last paragraph). It is known in the art that least-squares fit is compatible to root-mean square error minimization, when fitting a curve to a set of data.

69. Kim, Maxim, Dimopoulos, and Lancaster are analogous art because they are related to curve fitting.

70. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the root mean square error of Lancaster in the Kim–Maxim–Dimopoulos method because, when fitting a curve, Lancaster minimizes the sum of squared deviations (see page 44, last paragraph, lines 1–3), and as a result, Lancaster reports using a simpler function (see page 44, last paragraph, lines 8–9).

71. Claims 16–20, 22, 26–28, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim as applied to claim 29 above, taken in view of Reiss et al., (Reiss hereinafter), Spinelectronics And Its Applications.

72. As to claim 16, Kim discloses a method of simulating a memory device of an MTJ MRAM, the method comprising: calculating an indication of a first magnetic field and an indication of a second magnetic field applied to the MTJ (see page 898, col. 1, last two lines and col. 2, lines 1–8); detecting an indication of a transition of one of the first magnetic field and the second magnetic field across a threshold (see page 899, col. 1, lines 6–15); modifying a status of an operating condition of a plurality of operating conditions in response to the detecting the indication of a transition (see page 899, col. 1, lines 15–20); and providing an output bit state for the memory device, the output bit state is dependent upon a status of the plurality of operating conditions (see page 899, col. 1, lines 3–6).

73. While Kim discloses a method of simulating a memory device of an MTJ MRAM, Kim fails to disclose a method of simulating an MTJ MRAM with multiple free magnetic layers.

74. Reiss discloses a model of an MTJ MRAM with multiple free magnetic layers. (See page 292, last paragraph, lines 1–6 and page 301, Fig. 14).

75. Kim and Reiss are analogous art because they are both related to Spinelectronics and its applications.

76. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the model of Reiss in the method of Kim because Reiss studies how long-term Tunneling Magneto Resistance (TMR) behavior of tunnel junctions depends on the magnetic stability of the magnetically hard and soft electrodes (see page 301, next to last paragraph, lines 1–2), and as a result, Reiss reports improved efficiency of tunneling systems with an additional exchange bias layer (see page 301, 2nd paragraph, lines 1–3).

77. As to claim 17, Kim discloses a method wherein the plurality of operating conditions include a condition indicative of a presence of the first magnetic field above a predetermined threshold, a condition indicative of a presence of the second magnetic field above a predetermined threshold, a condition indicative of a presence of the first magnetic field above a predetermined threshold preceding a presence of the second magnetic field above a predetermined threshold, and a condition indicative of a presence of the second magnetic field above a predetermined threshold preceding a presence of the first magnetic field above a predetermined threshold (see page 899, col. 1, lines 11–15).

78. As to claim 18, Kim discloses a method further comprising: calculating a current conducted through the magnetic tunnel junction (MTJ) of the memory device based on a logic value of the bit state (see page 899, col. 1, lines 25–30).

79. As to claim 19, Kim discloses a method further comprising: modeling a conductance value of the MTJ in each of two bit states using an equation having an equivalent form of $G(A+BV+CV^2)$, where G is a conductance value of the MTJ, A, B,

and C are zero, first, and second order voltage coefficient parameters, and V is a MTJ bias voltage value (see page 899, col. 2, lines 6–12).

80. Claim 19 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 899, col. 2, lines 6–12) is functionally equivalent to the results produced by the step expressly claimed in Applicant's dependent claim 19. Therefore, the "product" that is produced by performing the step disclosed in dependent claim 8 is the functional equivalent of the "product" that is produced in (page 899, col. 2, lines 6–12). Although the "step" by which the end result is different, the final result for the "step" is identical.

81. As to claim 20, Kim discloses a method utilizing a first set of zero, first, and second order voltage coefficient parameters for the conductance value for a first bit state and utilizing a second set of, zero, first, and second order voltage coefficient parameters for the conductance value for a second bit state (see page 899, col. 2, lines 6–12).

82. Claim 20 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 899, col. 2, lines 6–12) is functionally equivalent to the results produced by the step expressly claimed in Applicant's dependent claim 20. Therefore, the "product" that is produced by performing the step disclosed in dependent claim 8 is the functional equivalent of the "product" that is produced in (page 899, col. 2, lines 6–12). Although the "step" by which the end result is different, the final result for the "step" is identical.

83. As to claim 22, Kim discloses a method further comprising: calculating A, B, and C as a function of temperature (see page 899, col. 2, lines 6–12).

84. As to claim 26, Kim discloses a method wherein the calculating an indication of a first magnetic field applied to the MTJ further includes calculating a first current in a first write conductor; the calculating an indication of a second magnetic field applied to the MTJ further includes calculating a second current in a second write conductor (see page 899, col. 1, lines 20–25) the first write conductor is disposed substantially orthogonal to the second write conductor with the MTJ disposed between the first write conductor and the second write conductor (see page 897, Fig. 1).

85. Claim 26 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 899, col. 1, lines 20–25) is functionally equivalent to the results produced by the step expressly claimed in Applicant's dependent claim 26. Therefore, the "product" that is produced by performing the step disclosed in dependent claim 8 is the functional equivalent of the "product" that is produced in (page 899, col. 1, lines 20–25). Although the "step" by which the end result is different, the final result for the "step" is identical.

86.

87. As to claim 27, Kim discloses a method wherein the calculating an indication of a first magnetic field applied to the MTJ further includes calculating the first magnetic field from the first current; the calculating an indication of a second magnetic field applied to the MTJ further includes calculating the second magnetic field from the second current (see page 899, col. 1, lines 20–25).

88. Claim 27 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 899, col. 1, lines 20–25) is functionally equivalent to the results produced by the step expressly claimed in Applicant's dependent claim 27. Therefore, the "product" that is produced by performing the step disclosed in dependent claim 8 is the functional equivalent of the "product" that is produced in (page 899, col. 1, lines 20–25). Although the "step" by which the end result is different, the final result for the "step" is identical.

89. As to claim 28, Kim discloses a method wherein the threshold is a first threshold corresponding to the first magnetic field exceeding a lower threshold while increasing (see page 899, col. 1, lines 9–15).

90. As to claim 38, Reiss discloses a model of an MTJ MRAM with multiple free magnetic layers. (See page 292, last paragraph, lines 1–6 and page 301, Fig. 14).

91. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim taken in view of Reiss as applied to claim 19 above, and further in view of Das.

92. As to claim 21, while the Kim–Reiss method for simulating an MTJ MRAM models a conductance value of the MTJ in each of two bit states, the Kim–Reiss method fails to utilize a first set of coefficients for the conductance value for a positive MTJ bias voltage and utilize a second set of coefficients for the conductance value for a negative MTJ bias voltage, in at least one of the two bit states.

93. Das discloses utilizing a first set of zero, first, and second order voltage coefficient parameters for the conductance value for a positive MTJ bias voltage and

utilizing a second set of zero, first, and second order voltage coefficient parameters for the conductance value for a negative MTJ bias voltage, in at least one of the two bit states. (See page 2890, col. 1, lines 18–22).

94. Claim 21 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the process disclosed in Das (page 2890, col. 1, lines 18–22) is functionally equivalent to the results produced by the steps expressly claimed in Applicant's independent claim 21. Therefore, the "product" that is produced by performing the steps disclosed in independent claim 5 is the functional equivalent of the "product" that is produced in Das (page 2890, col. 1, lines 18–22). Although the "process" by which the end result is different, the final result for the "process" is identical.

95. Kim, Reiss, and Das are analogous art because they are related to models for MTJ MRAM cells.

96. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the method of Das in the Kim–Reiss method because Das models the quasi-static hysteretic nature and thermal effects of an SDT device (see page 2889, col. 1, lines 25–28), and as a result, Das improves over his previous model for different types of giant magneto resistance (GMR) memory bits. (See page 2889, col. 1, lines 28–30).

97. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim taken in view of Reiss as applied to claim 19 above, and further in view of Maxim.

98. As to claim 23, while the Kim–Reiss method for simulating an MTJ MRAM models a conductance value of the MTJ in each of two bit states, the Kim–Reiss method fails to disclose generating values of G, A, B, and C by fitting low resistance state conductance data, high resistance state conductance negative bias voltage data, and high resistance state conductance positive bias voltage data for predetermined temperatures with second order polynomials; and fitting individual polynomial coefficient parameters to first order temperature polynomials.

99. Maxim discloses a method wherein values of G, A, B, and C are generated by a method comprising: fitting low resistance state conductance data, high resistance state conductance negative bias voltage data, and high resistance state conductance positive bias voltage data for predetermined temperatures with second order polynomials (see page 396, col. 1, lines 29–34); and fitting individual polynomial coefficient parameters to first order temperature polynomials (see page 397, col. 1, lines 3–14).

100. Kim, Reiss, and Maxim are analogous art because they are related to modeling of magnetic components.

101. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the Macro–modeling of Maxim in the Kim–Reiss method because Maxim achieves portability of his macro–model to SPICE simulators that do not support time integral (SDT) and time derivative (DDT) predefined ABM functions (see page 398, col. 2, lines 4–7), and as a result, Maxim reports a high computational efficiency with no convergence problems (see page 399, col. 1, last paragraph, lines 1–4).

102. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim taken in view of Reiss further in view of Maxim as applied to claim 23 above, and further in view of Dimopoulos.

103. As to claim 24, while the Kim–Reiss–Maxim method simulates an MTJ MRAM modeling a conductance value of the MTJ in each of two bit states, the Kim–Reiss–Maxim method fails to adjust one or more of the individual polynomial coefficient parameters to minimize a total error being measured between the second order polynomials and each of the low resistance state conductance data, the high resistance state conductance negative bias voltage data, and the high resistance state conductance positive bias voltage data.

104. Dimopoulos discloses adjusting one or more of the individual polynomial coefficient parameters to minimize a total error being measured between the second order polynomials and each of the low resistance state conductance data, the high resistance state conductance negative bias voltage data, and the high resistance state conductance positive bias voltage data (see page 146, Eq. 5.17; pages 152–154; page 160, lines 17–26; and page 161, line 1).

105. Kim, Reiss, Maxim and Dimopoulos are analogous art because they are related to magnetic tunnel junctions.

106. Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to utilize the error minimization of Dimopoulos in the Kim–Reiss–Maxim method because Dimopoulos fits experimental conductance curves for

magnetic tunnel junctions (see page 160, lines 4–6), and as a result, Dimopoulos reports that his model describes accurately experimental data for the conductance of magnetic tunnel junctions accounting for observed temperature variations (see page 161, lines 6–9).

107. As to claim 25, Maxim discloses a eliminating one or more of the polynomial coefficient parameters, which have a minimal effect on error being measured (see page 397, col. 1, next to last paragraph, lines 2 and 5–8).

108. Claim 25 has been given a broad reasonable interpretation by the Examiner. The Examiner notes that the step disclosed in (page 397, col. 1, next to last paragraph, lines 2 and 5–8) is functionally equivalent to the results produced by the step expressly claimed in Applicant's dependent claim 25. Therefore, the "product" that is produced by performing the step disclosed in dependent claim 25 is the functional equivalent of the "product" that is produced in (page 397, col. 1, next to last paragraph, lines 2 and 5–8). Although the "step" by which the end result is different, the final result for the "step" is identical.

Conclusion

109. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan C. Ochoa whose telephone number is (571) 272-2625. The examiner can normally be reached on 7:30AM - 4:00 PM.

110. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

111. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12/20/05

Paul L. Rodriguez 12/23/05

Primary Examiner
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